P. R. GOVERNMENT (A) COLLEGE, KAKINADA

DEPARTMENT OF COMPUTER SCIENCE

Virtual Class Delivered Programme

Activity : Virtual Class delivered Programm

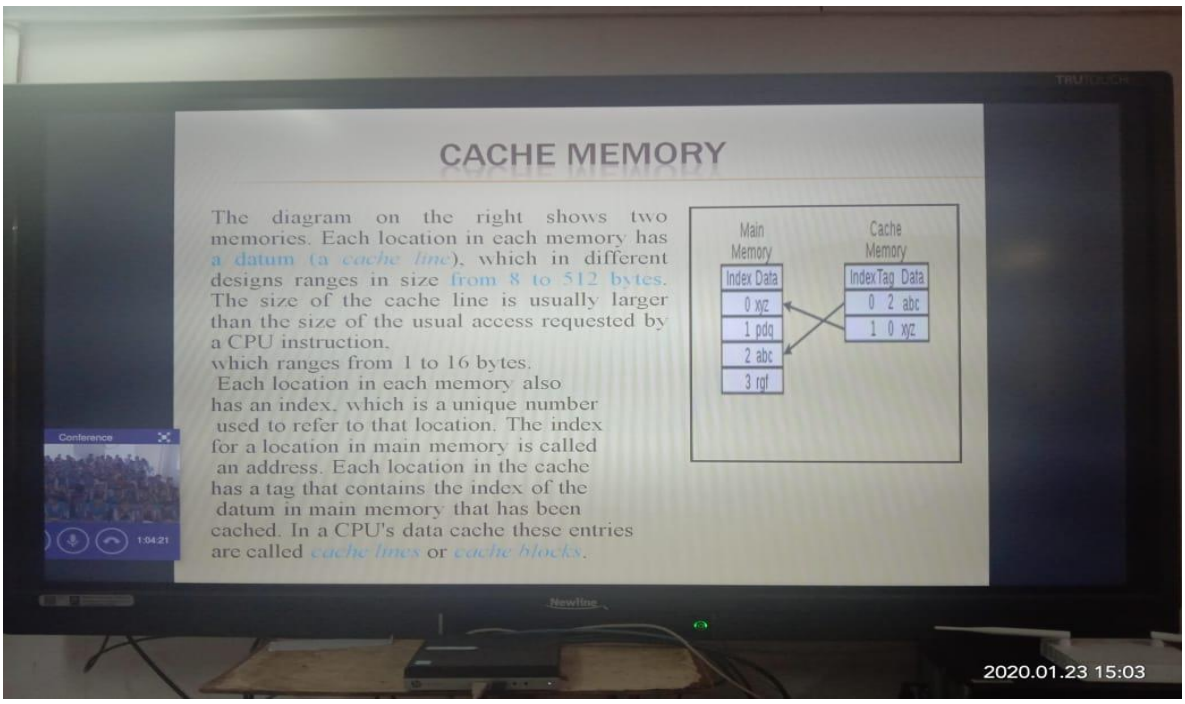
Conducted by : Department of Computer Science

Date : 23-01-2020

Topic : Classification of Memory (I BSc - CS)

Delivered virtual class lecturer by Sri R N Raghu Ram in Computer Science, at P R Govt College Kakinada.

PHOTOS THE OF ACTIVITY:


CACHE MEMORY
The diagram on the right shows two memories. Each location in each memory has a datum (a cache line), which in different designs ranges in size from 8 to 512 bytes. The size of the cache line is usually larger than the size of the usual access requested by a CPU instruction, which ranges from 1 to 16 bytes.
Each location in each memory also has an index, which is a unique number used to refer to that location. The index for a location in main memory is called an address. Each location in the cache has a tag that contains the index of the datum in main memory that has been cached. In a CPU's data cache these entries are called cache lines or cache blocks.
Main Memory
Index Data
0 xyz
1 pdq
2 abc
3 rgf
Cache Memory
Index Tag Data
0 2 abc
1 0 xyz
Conference
1:04:21
2020.01.23 15:03


BIDARAPUR RAJAJIPA GOVERNMENT COLLEGE